

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of: Ottmar Koeder ET AL.

Appln. No.: Not yet assigned

Filed: Herewith

For: METHOD FOR ALTERING  
 DESIGN DATA FOR  
 PRODUCING A COMPONENT,  
 AND ASSOCIATED UNITS

Examiner: Not yet assigned

Art Unit: N/A

Attorney Docket No: 10808/195

INFORMATION DISCLOSURE STATEMENT

In accordance with the duty of disclosure under 37 C.F.R. §1.56 and §§1.97-1.98, and more particularly in accordance with 37 C.F.R. §1.97(b), Applicants hereby cite the following reference(s):

| No.   | Date of Publication | Patentee/Applicant/Assignee |
|---|---------------------|-----------------------------|
| US 2001/0047507 A1  | November 29, 2001   | Pileggi et al.              |
| 6,363,519 B1  | March 26, 2002      | Levi et al.                 |
| 5,914,887   | June 22, 1999       | Scepanovic et al.           |
| 6,052,677   | April 18, 2000      | Masuoka et al.              |
| 6,360,191 B1  | March 19, 2002      | Koza et al.                 |
| <b>FOREIGN PATENT DOCUMENTS</b>   |                     |                             |
| DOCUMENT NUMBER<br><small>Number-Kind Code (if known)</small>   | DATE                | COUNTRY                     |
| EP 0431 532 A2  | June 12, 1991       | EPO                         |
| <b>OTHER ART – NON PATENT LITERATURE DOCUMENTS</b>  |                     |                             |
| Copy of International Search Report from International Application No. PCT/DE03/01863.  |                     |                             |
| Mehmet Aktuna, Rob A. Rutenbar and L. Richard Carley, "Device-Level Early Floorplanning Algorithms for RF Circuits" pgs. 375-388, IEEE 1999.  |                     |                             |
| T. Arslan, D.H. Horrack and E. Ozdemir, "Structural Cell-Based VLSI Circuit Design Using a Genetic Algorithm" pgs.308-311, IEEE 1996.   |                     |                             |
| N. Zhuang, M.S.T. Bente and P.Y.K. Cheung, "Improved Variable Ordering of BDDS With Novel Genetic Algorithm" pgs. 414-417, IEEE 1996.   |                     |                             |
| Akio Sakamoto, Xingzhao Liu and Takashi Shimamoto, "A Modified Genetic Channel Router" pgs. 2076-2083, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences E77-A, No. 2, December 1994. |                     |                             |
| Imtiaz Ahmad, Muhammad Khan Dhodhi and Frank H. Hielscher, "Design-Spaced Exploration for High-Level Synthesis" pgs. 491-496, IEEE 1994.  |                     |                             |
| Ernest S. Kuh and Tatsuo Ohtsuki, "Recent Advances in VLSI Layout" pgs. 237-263, Vol.   |                     |                             |

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| David J. Powell, Siu Shing Tong and Michael M. Skolnick, "Domain Independent, Machine Learning for Design Optimization" pgs. 151-159, Proceeding of the Third International Conference on Genetic Algorithms, June 1989. |
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| Daniel Brand, "Hill Climbing with Reduced Search Space" pgs. 294-297, IEEE 1988. |
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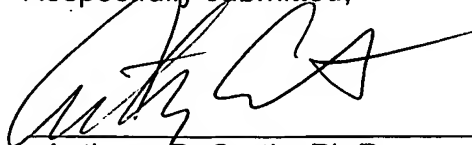
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| Mario P. Vecchi and Scott Kirkpatrick, "Global Wiring by Simulated Annealing" pgs. 215-222, Vol. CAD-2, No. 4, IEEE October 1983. |
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Applicants are enclosing Form PTO-1449 (two sheets), along with a copy of each listed reference for which a copy is required under 37 C.F.R. §1.98(a)(2). As each of the listed references is in English, no further commentary is believed to be necessary, 37 C.F.R. §1.98(a)(3). Applicants respectfully request the Examiner's consideration of the above reference(s) and entry thereof into the record of this application.

For purposes of 37 C.F.R. §1.704(d), Applicant certifies that each item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart application. By submitting this Statement, Applicants are attempting to fully comply with the duty of candor and good faith mandated by 37 C.F.R. §1.56. As such, this Statement is not intended to constitute an admission that any of the enclosed references, or other information referred to therein, constitutes "prior art" or is otherwise "material to patentability," as that phrase is defined in 37 C.F.R. §1.56(a).

Applicants have calculated no fee to be due in connection with the filing of this Statement. However, the Director is authorized to charge any fee deficiency associated with the filing of this Statement to a deposit account, as authorized in the Transmittal accompanying this Statement.

Respectfully submitted,



Anthony P. Curtis, Ph.D.  
(Reg. No. 46,193)

12/16/04  
Date

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| FORM PTO-1449  | SERIAL NO. <b>107518291</b><br>Not yet assigned 10808/195                                     |
| LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT<br>(use several sheets if necessary) | FILING DATE Herewith<br>GROUP ART UNIT Not yet assigned<br>APPLICANT(S): Ottmar Koeder et al. |

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

| EXAMINER INITIAL |    | DOCUMENT NUMBER<br>Number-Kind Code (if known) | DATE              | NAME              | CLASS/<br>SUBCLASS | FILING DATE |
|------------------|----|--|-------------------|-------------------|--------------------|-------------|
|                  | A1 | US 2001/0047507 A1                             | November 29, 2001 | Pileggi et al.    |                    |             |
|                  | A2 | 6,363,519 B1                                   | March 26, 2002    | Levi et al.       |                    |             |
|                  | A3 | 5,914,887                                      | June 22, 1999     | Scepanovic et al. |                    |             |
|                  | A4 | 6,052,677                                      | April 18, 2000    | Masuoka et al.    |                    |             |
|                  | A5 | 6,360,191 B1                                   | March 19, 2002    | Koza et al.       |                    |             |
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## FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL |    | DOCUMENT NUMBER<br>Number-Kind Code (if known) | DATE          | COUNTRY | CLASS/<br>SUBCLASS | TRANSLATION<br>YES OR NO |
|------------------|----|--|---------------|---------|--------------------|--------------------------|
|                  | A6 | EP 0431 532 A2                                 | June 12, 1991 | EPO     |                    |                          |
|                  |    |  |               |         |                    |                          |
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|                  |    |  |               |         |                    |                          |
|                  |    |  |               |         |                    |                          |

| EXAMINER INITIAL | OTHER ART – NON PATENT LITERATURE DOCUMENTS<br>(Include name of author, title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date page(s), volume-issue number(s), publisher, city and/or country where published.) |   |
|------------------|--|---|
|                  | A7   | Copy of International Search Report from International Application No. PCT/DE03/01863.  |
|                  | A8   | Mehmet Aktuna, Rob A. Rutenbar and L. Richard Carley, "Device-Level Early Floorplanning Algorithms for RF Circuits" pgs. 375-388, IEEE 1999.  |
|                  | A9   | T. Arslan, D.H. Horrack and E. Ozdemir, "Structural Cell-Based VLSI Circuit Design Using a Genetic Algorithm" pgs.308-311, IEEE 1996.   |
|                  | A10  | N. Zhuang, M.S.T. Benten and P.Y.K. Cheung, "Improved Variable Ordering of BDDS With Novel Genetic Algorithm" pgs. 414-417, IEEE 1996.  |
|                  | A11  | Akio Sakamoto, Xingzhao Liu and Takashi Shimamoto, "A Modified Genetic Channel Router" pgs. 2076-2083, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences E77-A, No. 2, December 1994. |
|                  | A12  | Imtiaz Ahmad, Muhammad Khan Dhodhi and Frank H. Hielscher, "Design-Spaced Exploration for High-Level Synthesis" pgs. 491-496, IEEE 1994.  |
| EXAMINER         |  | DATE CONSIDERED   |

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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| FORM PTO-1449  | SERIAL NO.<br>Not yet assigned     | CASE NO.<br><b>10/518291</b><br>10808-195 |
| <b>LIST OF PATENTS AND PUBLICATIONS FOR<br/>APPLICANT'S INFORMATION DISCLOSURE<br/>STATEMENT</b> | FILING DATE<br>Herewith            | GROUP ART UNIT<br>Not yet assigned        |
| (use several sheets if necessary)  | APPLICANT(S): Ottmar Koeder et al. |   |

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|---------------------|---|--|
|                     | A13   | Ernest S. Kuh and Tatsuo Ohtsuki, "Recent Advances in VLSI Layout" pgs. 237-263, Vol. 78, No. 2, IEEE 1990.  |
|                     | A14   | David J. Powell, Siu Shing Tong and Michael M. Skolnick, "Domain Independent, Machine Learning for Design Optimization" pgs. 151-159, Proceeding of the Third International Conference on Genetic Algorithms, June 1989. |
|                     | A15   | Daniel Brand, "Hill Climbing with Reduced Search Space" pgs. 294-297, IEEE 1988.   |
|                     | A16   | Mario P. Vecchi and Scott Kirkpatrick, "Global Wiring by Simulated Annealing" pgs. 215-222, Vol. CAD-2, No. 4, IEEE October 1983.  |

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